

Agenda

Philips / Commodore Meeting

15 April 1994

- 9:00 Introductions / Organizations and Objectives
 Commodore / Philips
- 9:15 Commodore Products and Technology Roadmap
 Commodore: Lew Eggebrecht
- 10:30 HOMBRE Overall Goals and Strategy
 Commodore: Ed Hepler
- 11:00 HOMBRE Needs
 Commodore: Allan Havemose
- 11:30 HOMBRE Chip Set and System Configurations
 Commodore: Ed Hepler
- 12:00 Lunch
- 1:00 HOMBRE Chip Set Details
 Commodore: Ed Hepler
- 2:00 HOMBRE Software Details
 Commodore: Allan Havemose
- 3:00 HOMBRE Performance Estimates
 Commodore: Allan Havemose / Ed Hepler
- 3:30 Discussion / Wrapup
 Commodore: Lew Eggebrecht

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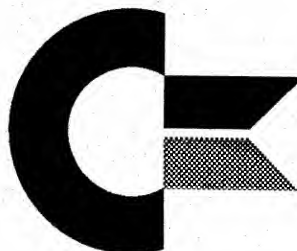
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Hombre Goals

- **Produce the Next Generation Product Family**
 - RISC Processor based
- **Direct Support for 3D Animation**
- **Define a Clean Architecture**
- **Target Wide Product Line**
- **Dovetail with higher end architecture**

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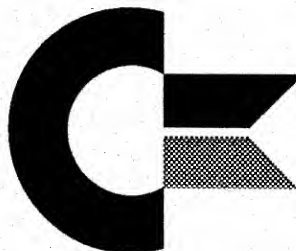
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Ground Rules

- **Late 1994 "First Silicon" Availability for 1995 Production**
 - Must be a player in the Christmas 1995 offerings
- **Cost effective solution**
 - Chip Set < \$40.00
 - Low-end to have 32-bit memory
 - Execute out of display memory
- **Flexible enough to support a number of products**
 - CD based Game Machine
 - Cable TV Set Top Box
 - MPEG Player
 - Home Computer
 - PCI based Graphics Accelerator
 - Desktop or Tower Based System
- **Target 0.6 micron - 3 level metal CMOS - 3.3 Volt process**

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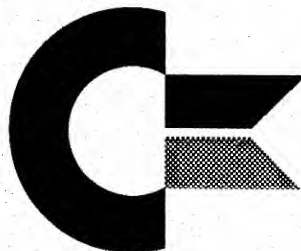
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Observations

- **Rendering is different for photorealistic imaging versus real-time animation**
- **Various levels of detail required**
 - Some portions of image relatively stable over many frames
 - Other portions change on a frame-by-frame basis
 - Only application (programmer) knows for sure
 - Trade-off detail with computational requirements
- **16-bit pixels are good enough**
- **Multiple playfields are useful**
- **Software Developers either want *many* sprites or none...**

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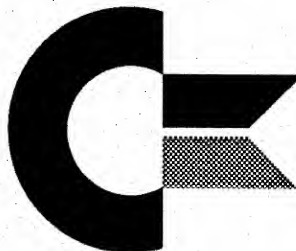
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Hombre Implementation Strategy

- **Select a RISC architecture to base the system upon:**
 - **Business/Competitive Issues**
 - Number of other implementations using processor family?
 - Would we be playing into the hands of a competitor (or potential competitor)?
 - Are there complementary systems to fill out high end?
 - **Performance Issues**
 - Code Density
 - Support for graphics operations, etc.
 - Support Chip(s) required (cache) to achieve performance
 - Bus Size required to achieve performance
 - **Implementation Issues**
 - Ease of implementing Integer Core with other functions
 - Ability to add customized instructions
 - **Cost Issues**
 - License fees?
 - Chip costs
- **Integrate RISC Integer Core with key system functions**
- **Build 2 or 3 chip low end system**

Use commercial RISC chip as add-in performance enhancer with low end, chip-set based system as intelligent peripheral sub-system

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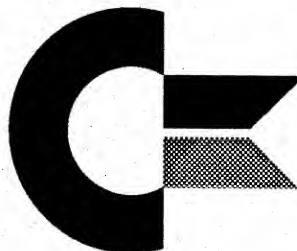
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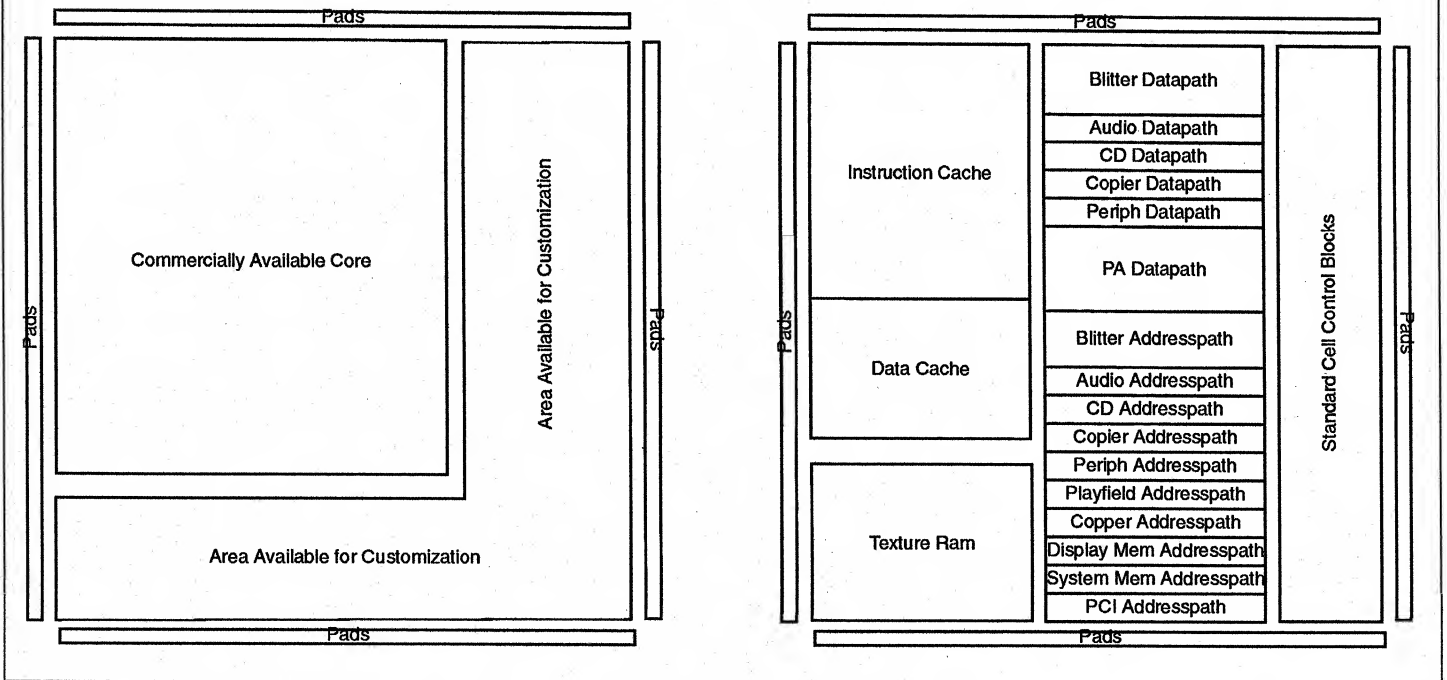
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Why an Embedded Processor?

- **Reduced Chip count should produce a reduced cost.**
- **Desire multiple simultaneous memory access paths:**
 - Graphics Update
 - Blitter, other DMA access
 - CPU fetches

Why Design our own core?

- **Ability to add instructions for graphics**
- **Easier to “mate” to other functional units**
- **Ability to control aspect ratio and positioning of blocks**



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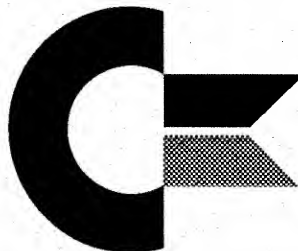
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Why PA-RISC?

- **Performance is very high compared to other RISC processors at similar clock rates.**
- **Code density enhanced by:**
 - **Powerful instruction set**
 - **Nullification**
 - **Atomic modification of addresses during load/stores**
- **SFU instruction expansion capability**
- **Demonstrated Low Cost Implementation**
- **Growth Path for future enhancements**
- **HP's operating system availability**
 - **UNIX**
 - **Windows/NT**
- **HP has a line of PA-RISC workstations which complement Commodore's offerings**
- **Development Tools available**
 - **GNU Tools available via ftp (we already have them...)**
 - **HP has its own software development tools**
 - **Can use HP workstations as cross-development platforms**

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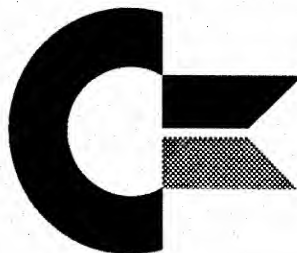
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RISC Code Comparison (Addr Mod)

From: Jim Hull and Martin Whittaker, "The Advantages of the PA-RISC Architecture In Embedded Control Applications"

```
int max, temp, value[100], *ptr;
```

```
max= 0;
for(ptr= value; ptr < value + 100; ) {
    temp= *ptr++;
    if(max < temp) {
        max= temp;
    }
}
```

PA-RISC

```
ldo    -56(%r30),%r23 ; r23= value+100
ldo    -456(%r30),%r31 ; ptr= value
copy   %r0,%r25      ; max= 0
ldws,ma 4(0,%r31),%r24 ; temp= *ptr++

loop:  comclr,>= %r25,%r24,%r0 ; if(max >= temp) nullify
copy   %r24,%r25      ; max= temp
comb,<<,n,%r31,%r23,loop ; if((ptr<value+100) loop
ldws,ma 4(0,%r31),%r24 ; temp= *ptr++ (next)
```

SPARC

```
add    %fp,-400,%i5 ; ptr= value
mov     0,%i3        ; max= 0
ld      [%i5],%i4    ; temp= *ptr

ly2:   inc 4,%i5      ; ptr++
cmp     %i3,%i4      ; if(max >= temp)
bge,a ly3            ; branch to end
cmp     %i5,%fp      ; if(ptr < value + 100)
mov     %i4,%i3      ; max= temp
cmp     %i5,%fp      ; temp= *ptr (next)

ly3:   bcs,a ly2      ; if(ptr < value+100) loop
ld      [%i5],%i4    ; temp= *ptr
```

MIPS

```
addiu r24,sp,32      ; ptr= value
addiu r2,sp,432      ; r4= value+ 100
move r3,r24          ; r3= ptr
move r5,r0           ; max= 0

$32: lw r2,0(r3)      ; temp= *ptr
addiu r3,r3,4        ; ptr++
slt r1,r5,r2          ; check if max < temp
beq r1,r0,$33        ; if not,br to end
sltu r1,r3,r4         ; check if ptr < value+100
move r5,r2           ; max= temp
sltu r1,r3,r4         ; check if ptr < value+ 100

$33: bne r1,r0,$32    ; if ptr < value, loop
nop                  ; nop in delay slot
```

Instruction Count	PA-RISC	SPARC	MIPS	68030
Static	8 (32 bytes)	11 (44 bytes)	13 (52 bytes)	? (22 bytes)
Dynamic	404	803	904	

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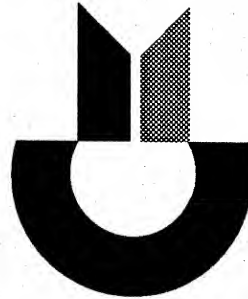
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RISC Code Comparison (Nullification)

From: Jim Hull and Martin Whittaker, "The Advantages of the PA-RISC Architecture In Embedded Control Applications"

```
proc(value, limit, alarm, overload)
int value, limit, *alarm, *overload; {

    if(value > limit) {
        *alarm= 1;
        *overload= value;
    } else {
        *alarm= 0;
    }
}
```

PA-RISC

```
comb,<=,n,%r26,%r25,ELSE; if(value <= limit) br
ldi 1,%r31 ; *alarm= 1
stws %r31,0(0,%r24) ; store to memory
bv 0(%r2) ; return
stws %r26,0(0,%r23) ; *overload= value

ELSE: bv 0(%r2) ; return
stws %r0,0(0,%r24) ; *alarm= 0;
```

SPARC

```
cmp %o0,%o1 ; test if (value <= limit)
ble,a LE33 ; branch to ELSE
st %g0,[%o2] ; if br, *alarm= 0
mov 1,%o4 ; *alarm= 1
st %o4,[%o2] ; store to memory
st %o0,[%o3] ; *overload= value

LE33: retl ; return
nop ; nop in delay slot
```

MIPS

```
slt r1,r4,r3 ; test if value <= limit
beq r1,r0,ELSE ; branch to ELSE
nop ; nop in delay slot
li r14,1 ;
sw r14,0(r5) ; *alarm= 1
jr r31 ; *overload= value

ELSE: sw r0,0(r5) ; *alarm= 0
jr r31 ; return
nop ; nop in delay slot
```

Instruction Count	PA-RISC	SPARC	MIPS
Static	7	8	10
Dynamic value > limit	5	8	7
Dynamic value <= limit	4	5	6

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Hombre Function Partitioning

CPU Chip

PA-RISC Integer Core with MMU/Cache
Blitter (Raster-ops, Lines, Fills (Textured, Shaded))
Copper (Video Line synchronized)
Audio (AAA style, with serial inputs and outputs)
CD-ROM interface
Memory Block copy
Peripheral Bus Interface (4 8-bit peripherals)
DMA Control
Real time clock and interval timer
External Processor Interface
PCI bus interface
DRAM/VRAM controllers

Video Chip

Playfield Line buffers
Cursor Memory
Horizontal and Vertical Video Counters
Monitor Control
Video Output Logic
Color Lookup Table
Mouse/Joystick Logic
Genlock, Sampling Logic

- Amiga-like functionality will ease transition
- Bonding Options for lower cost packaging

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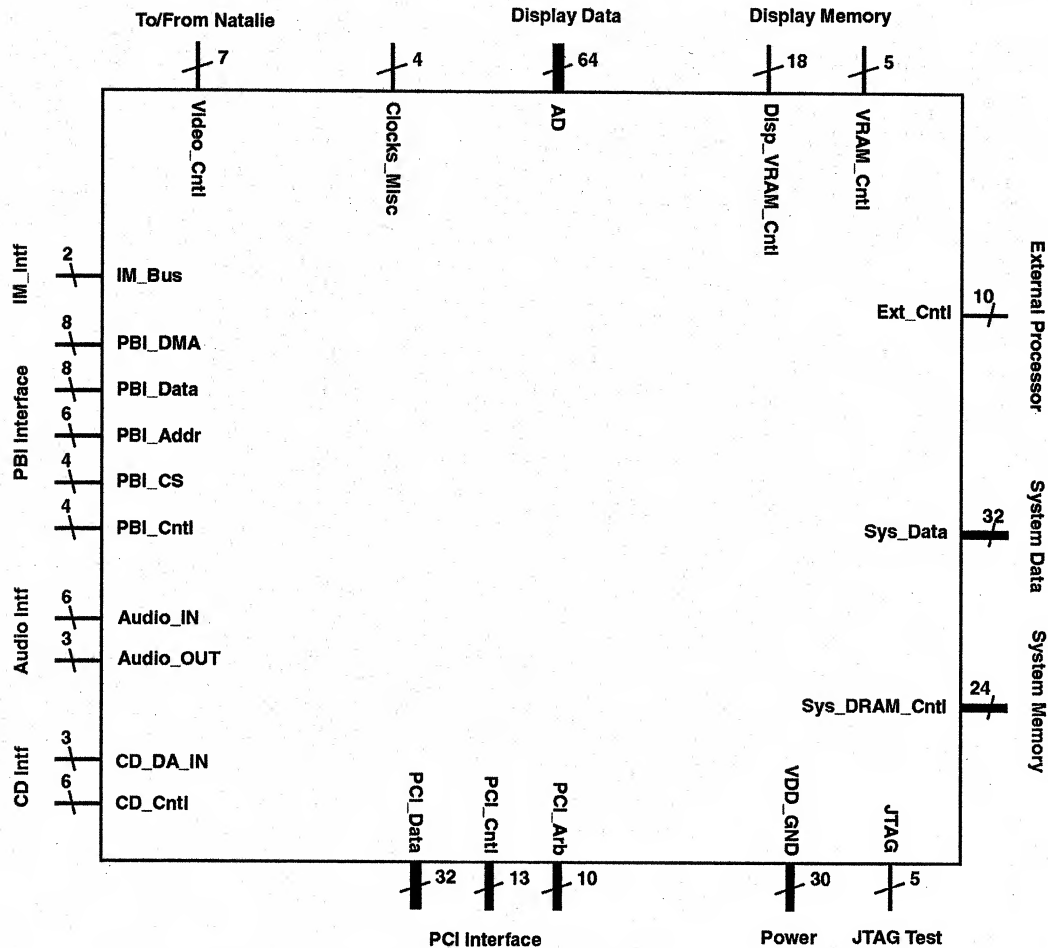
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CPU/Rendering Chip (Nathaniel)



• Functions:

- RISC Int. Core (MMU/Cache)
- Blitter/Renderer
- 8-bit DMA Interface
- Audio Processor
- CD-ROM Interface
- PCI Bus
- Memory Copier
- Copper

• Interfaces:

- 32/64-bit Display Memory Interface
- 32-bit System Memory Interface
- 32-bit PCI Interface
- 8-bit Peripheral Bus Interface
- 2-bit IM Bus Interface
- 274 Signals / 30 Power-Ground
- 304 PQFP (313 BGA)

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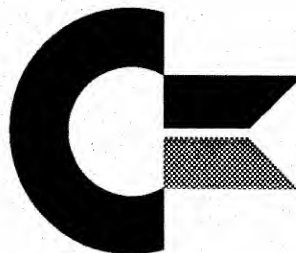
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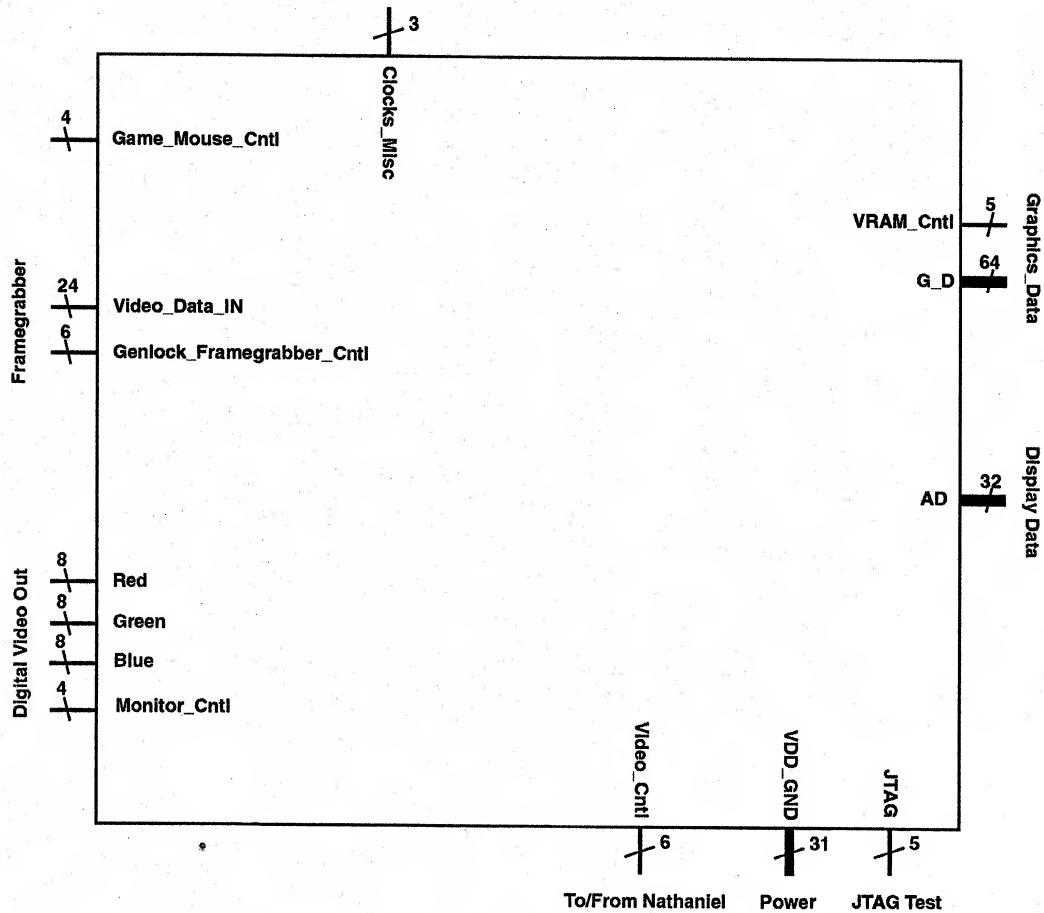
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Video Chip (Natalie)



• Functions:

- Line Buffers
- Cursor Ram
- 512 x 25 CLUT
- Framegrabber
- Genlock
- YUV -> RGB (MPEG)
- Mouse/Game Cntrlr Intf

• Interfaces:

- 32/64-bit Graphics Data (VRAM)
- 32-bit Display Memory (high 32)
- 24-bit Digital RGB out (ext D/A)
- 24-bit (option to 8+16) Video IN
- Serial Mouse - Game Control

- 177 Signals / 31 Power-Ground
- 208 PQFP (225 BGA)

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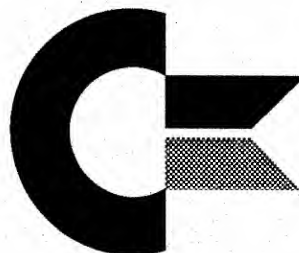
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Multiple Products from a Single Chip Set

- **CD based Game Machine**
- **Cable TV Set Top Box**
- **MPEG Player**
- **Home Computer**
- **PCI based Graphics Accelerator**
- **Desktop or Tower Based System**

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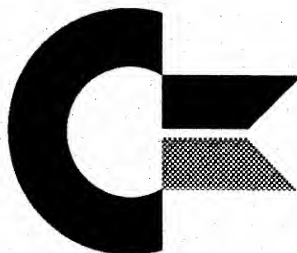
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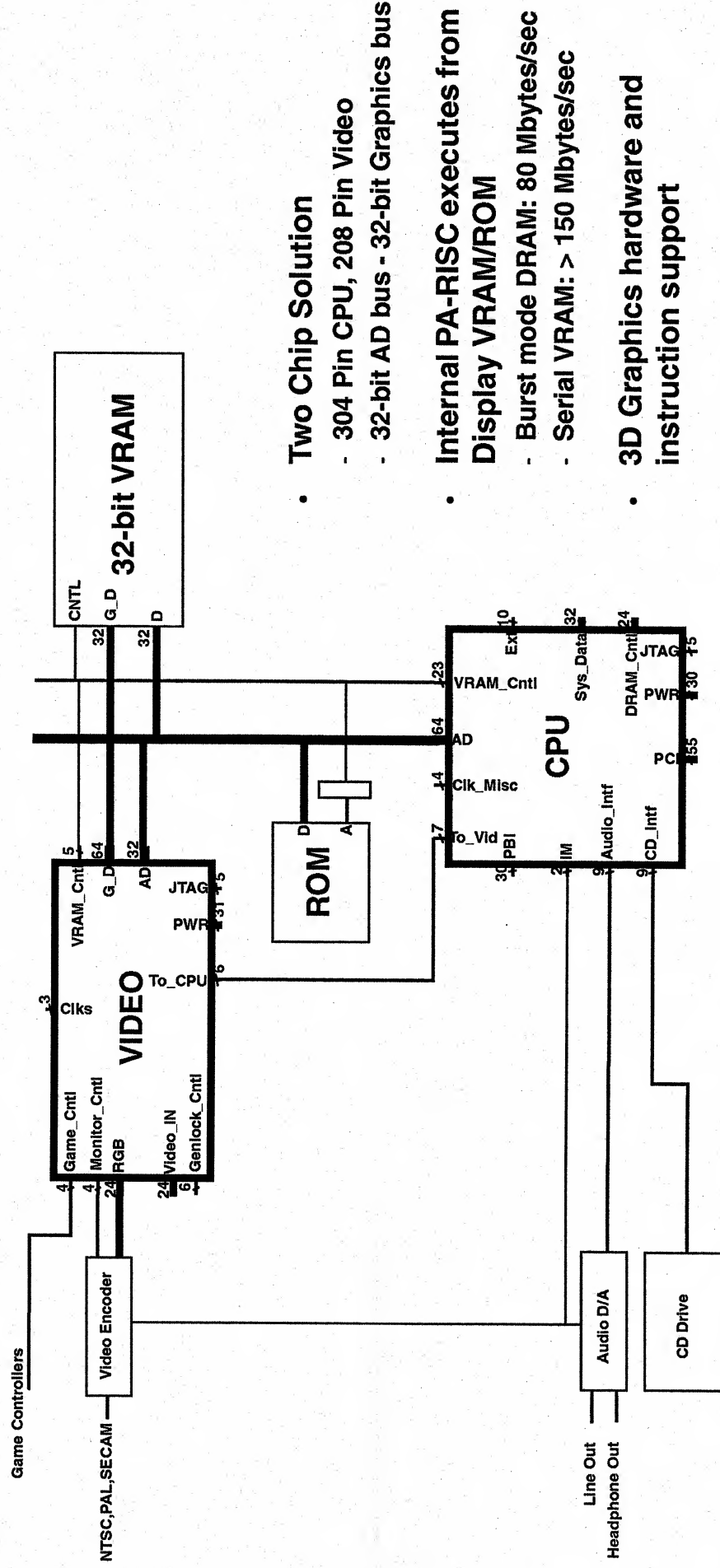


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Next Generation CD based Game Machine (Minimal)



- **Two Chip Solution**
 - 304 Pin CPU, 208 Pin Video
 - 32-bit AD bus - 32-bit Graphics bus
- **Internal PA-RISC executes from Display VRAM/ROM**
 - Burst mode DRAM: 80 Mbytes/sec
 - Serial VRAM: > 150 Mbytes/sec
- **3D Graphics hardware and instruction support**

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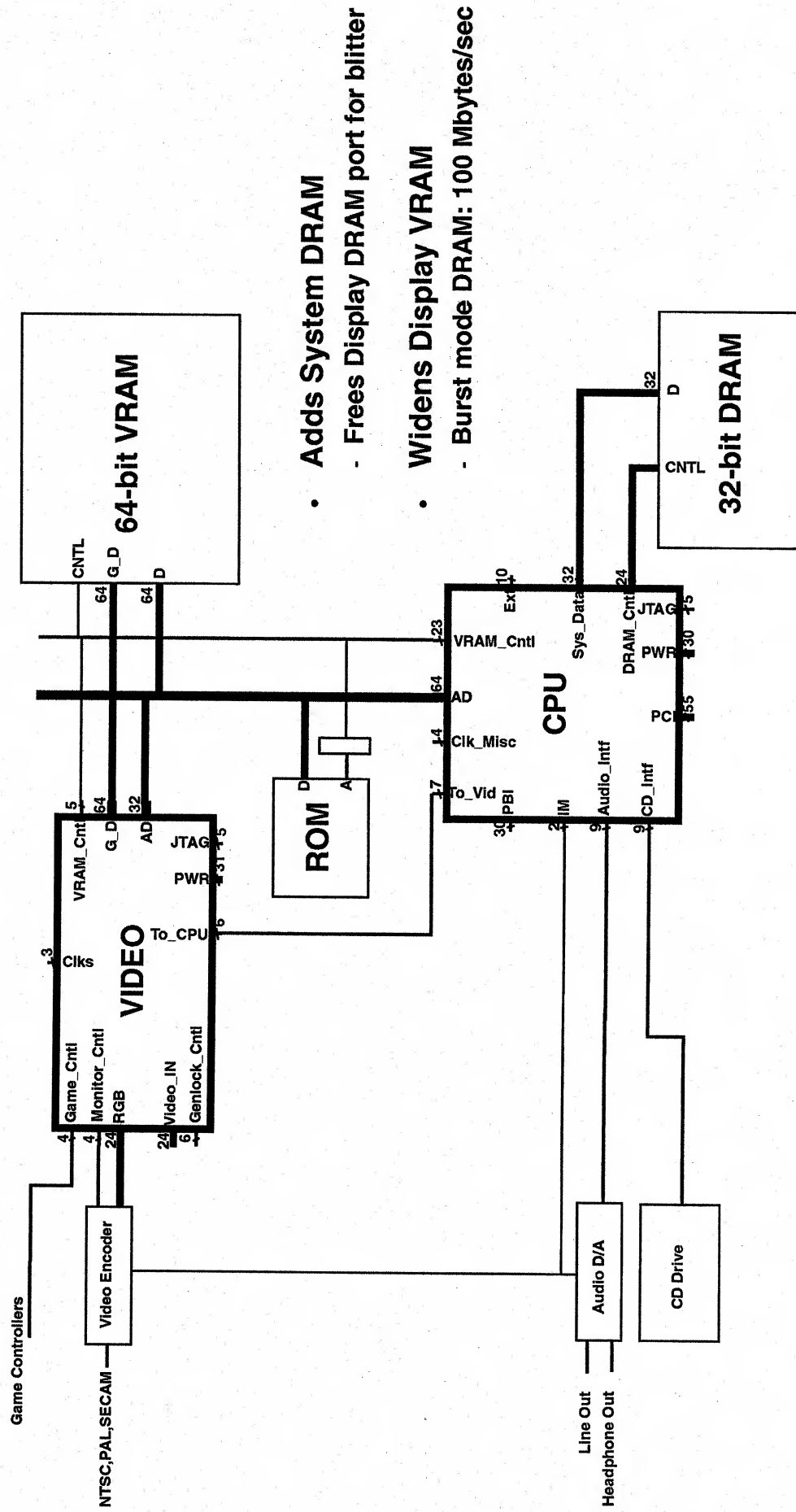


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Next Generation CD based Game Machine (Expanded)



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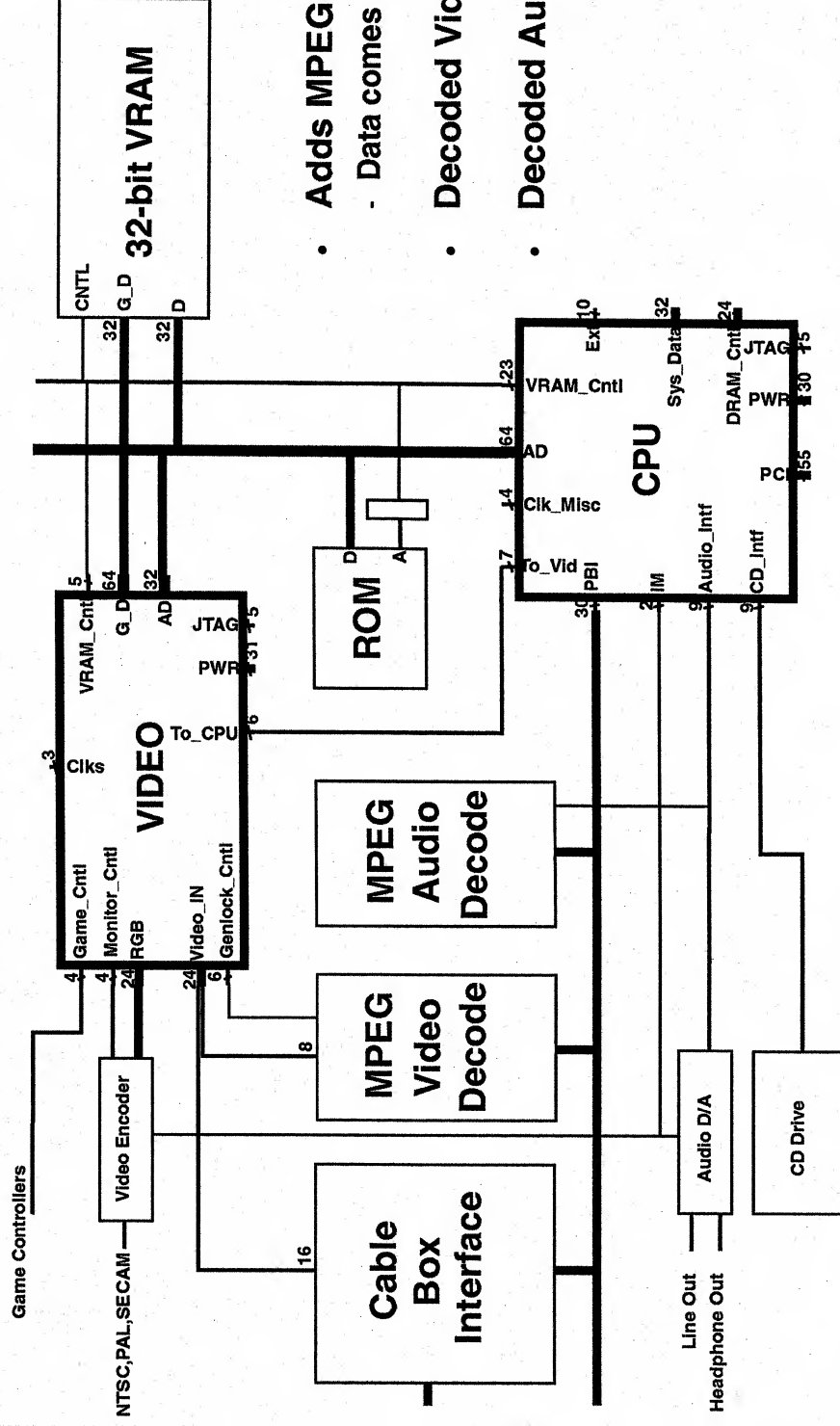
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MPEG Player or Cable Box (Minimal)



- Adds MPEG Intf via PBI
 - Data comes from CD or Cable Intf
- Decoded Video merged in Video Chip
- Decoded Audio merged in CPU Chip

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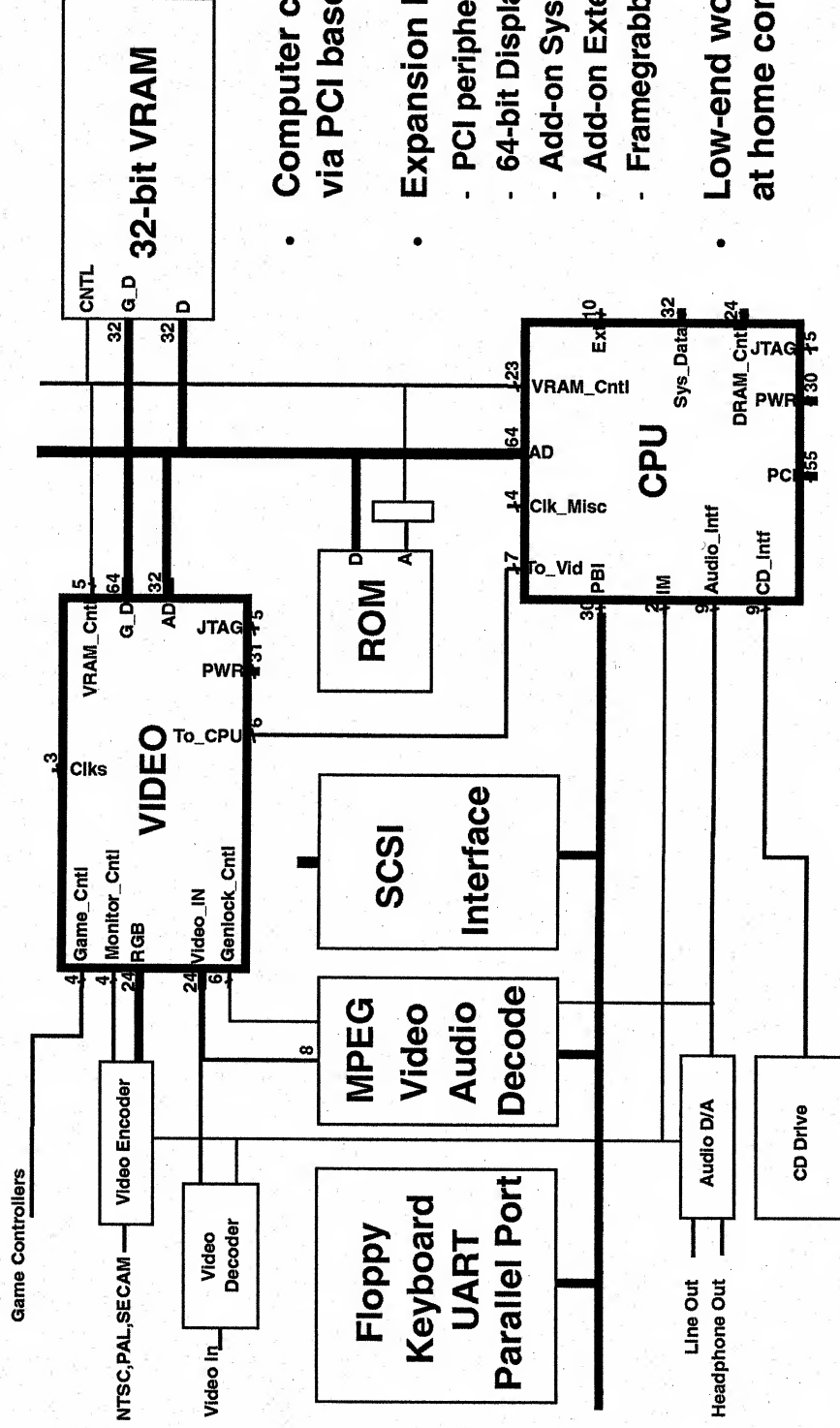
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A1200 Class Home Computer (via PBI)



- Computer could also be achieved via PCI based ASIC
- Expansion Possible:
 - PCI peripherals
 - 64-bit Display VRAM
 - Add-on System DRAM
 - Add-on External Processor
 - Framegrabber
- Low-end workstation performance at home computer costs

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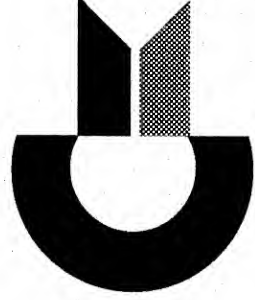
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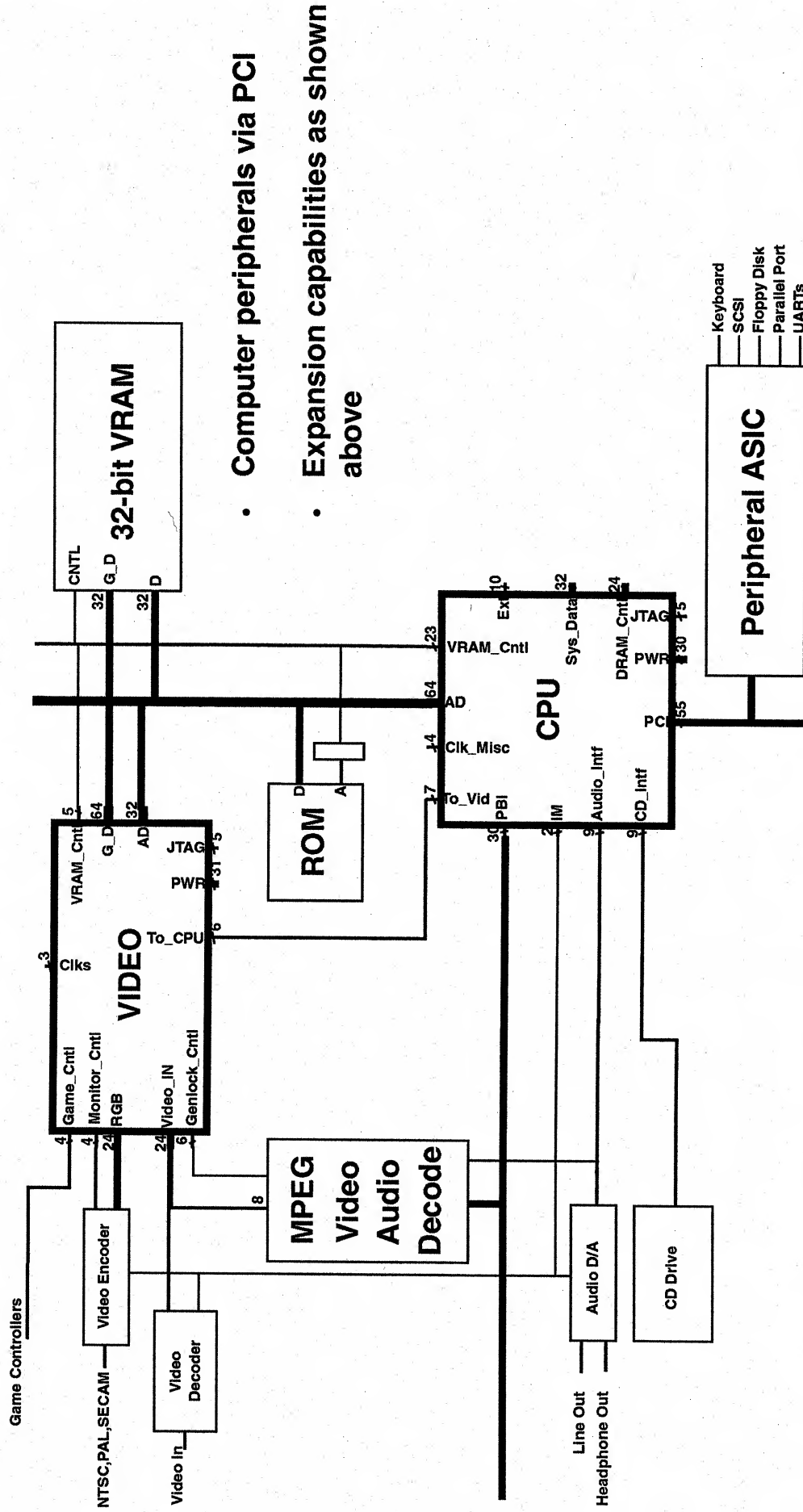
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A1200 Class Home Computer (via PCI)



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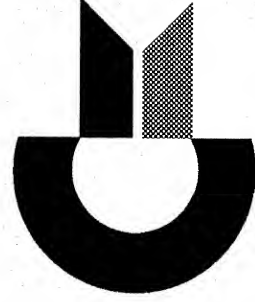
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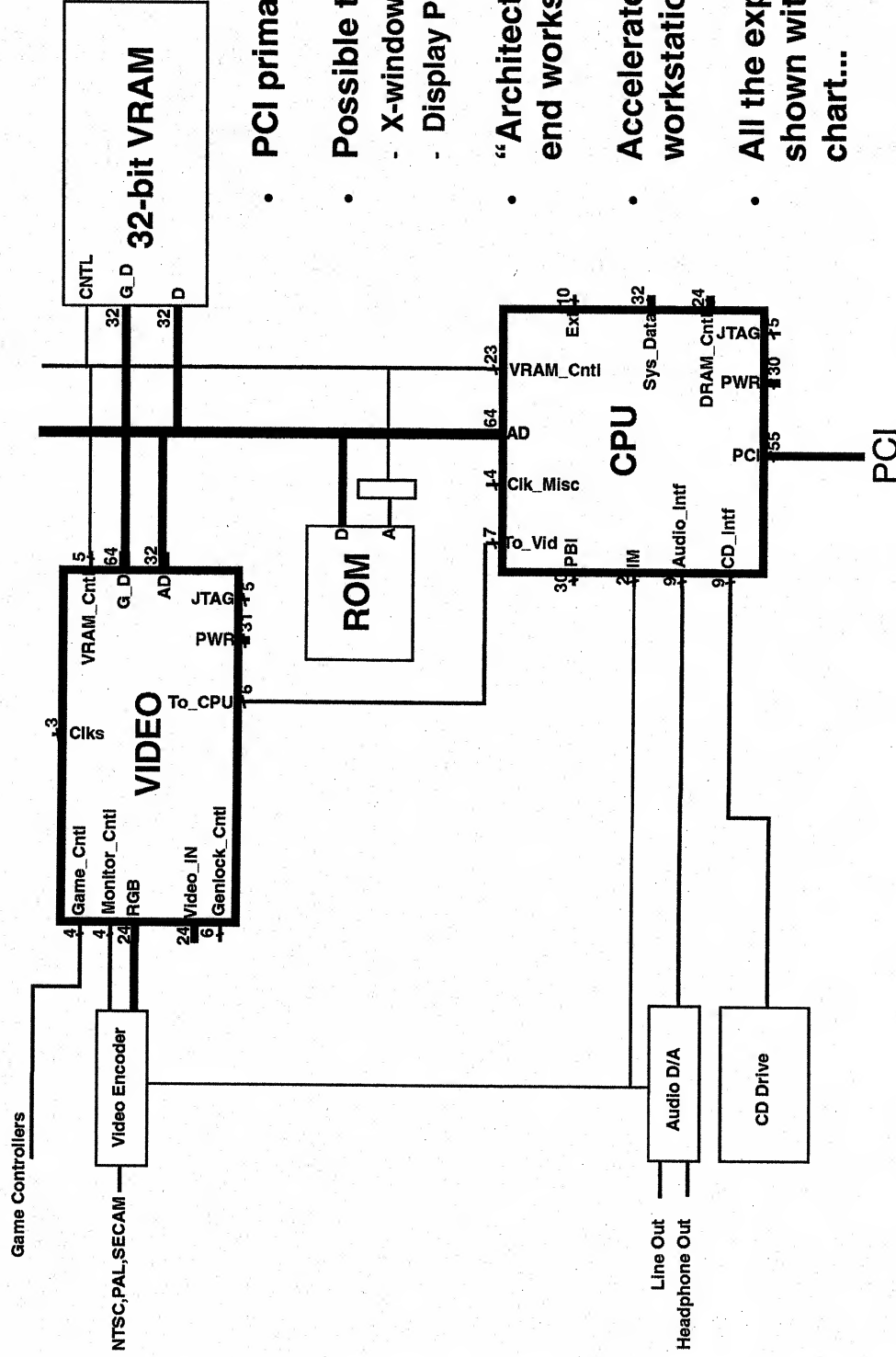
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Multimedia Graphics Accelerator



- PCI primarily slave interface
- Possible to "download" code
 - X-windows driver
 - Display PostScript Interpreter
- "Architectural-Link" to HP high-end workstations
- Accelerator for PC or MAC workstations
- All the expansion possibilities shown with the home computer chart...

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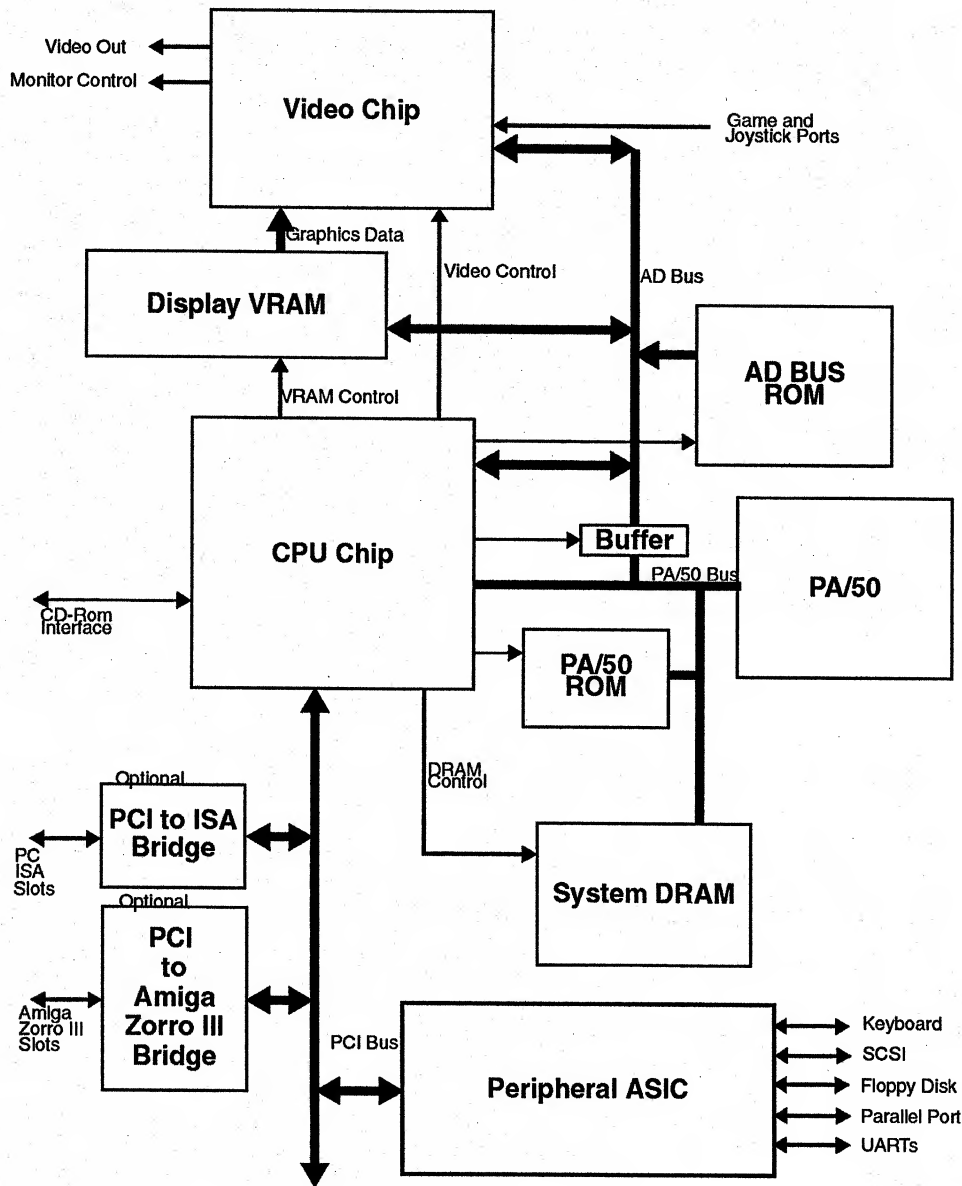
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Desktop and/or Tower Systems



- Ext. PA/50 Proc., Additional DRAM, and Bus intf. added

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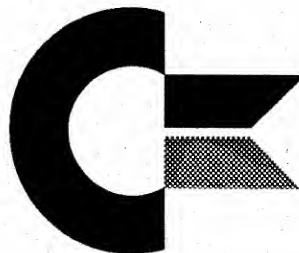
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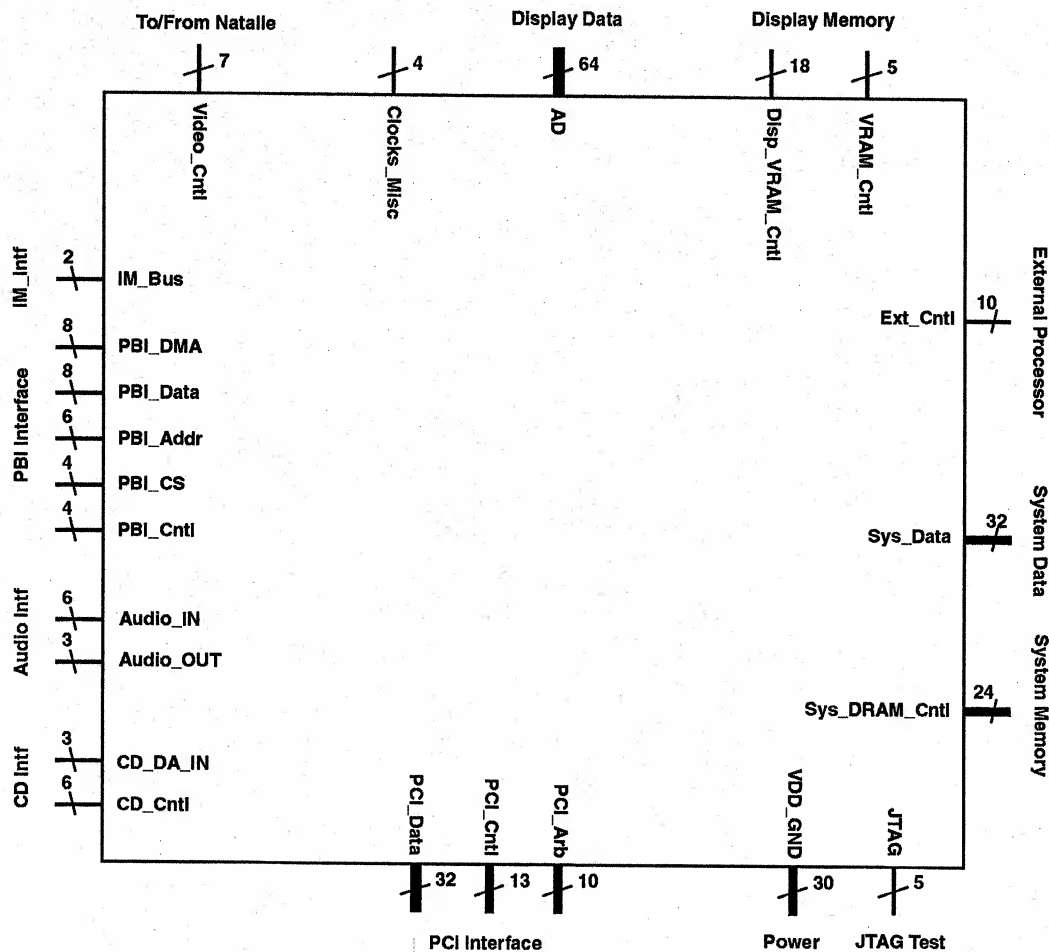


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CPU/Rendering Chip (Nathaniel)



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- Memory Copier
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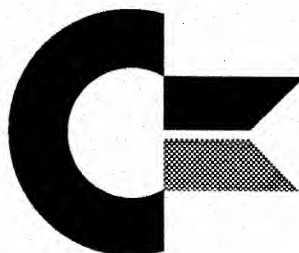
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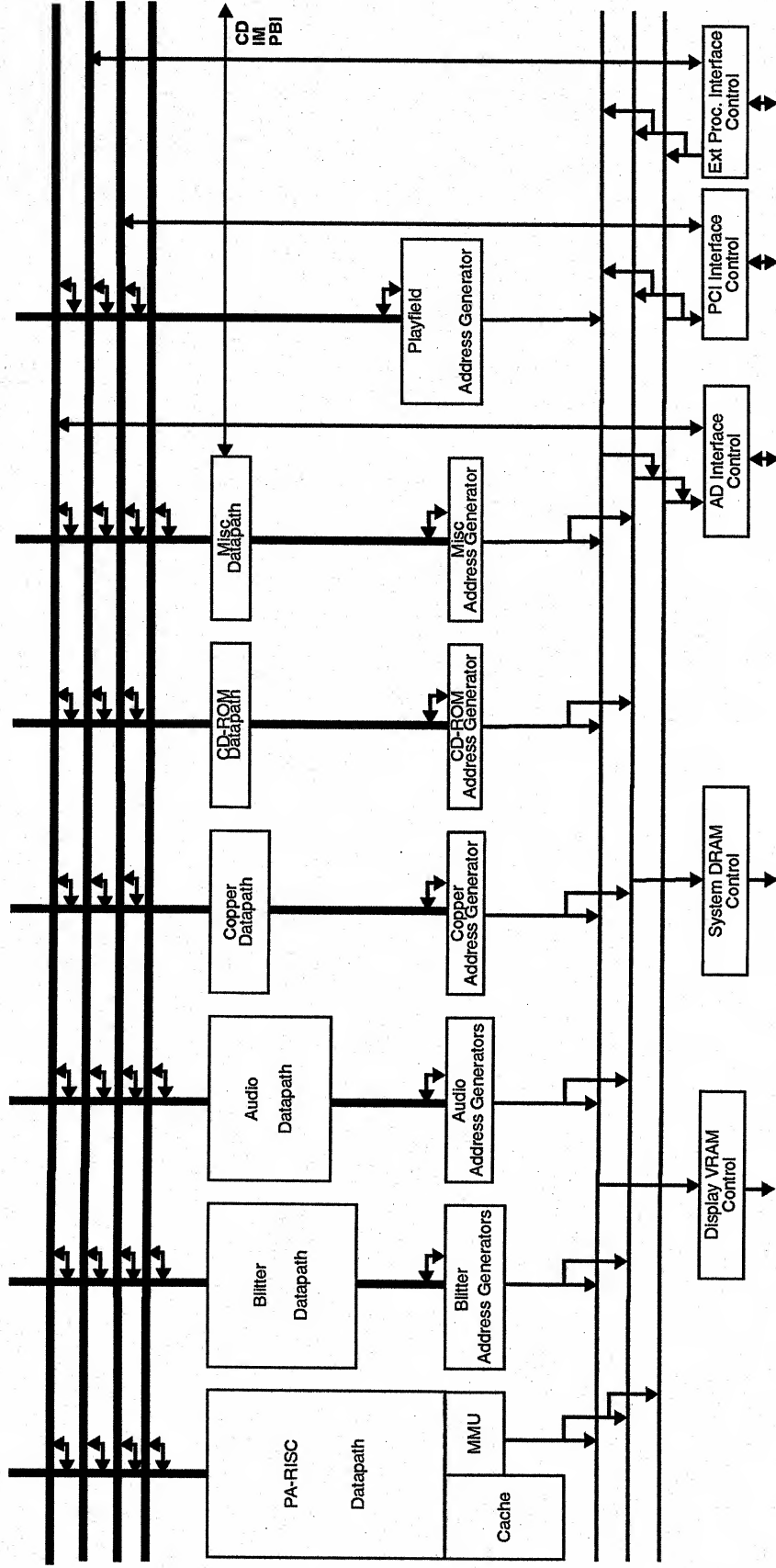


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Functional Block Diagram of CPU



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PA-RISC Implementation

- **Level 1 implementation - Integer only**
- **5 Stage Integer Pipeline**
- **Datapath widened to 64 bits**
 - Even-odd register pairs may be accessed
- **Execution Stage includes graphics functional unit**
- **Would like to add support for simple floating point functions.**

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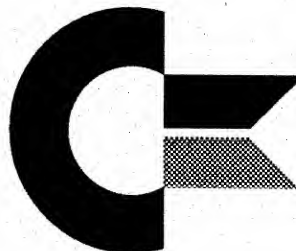
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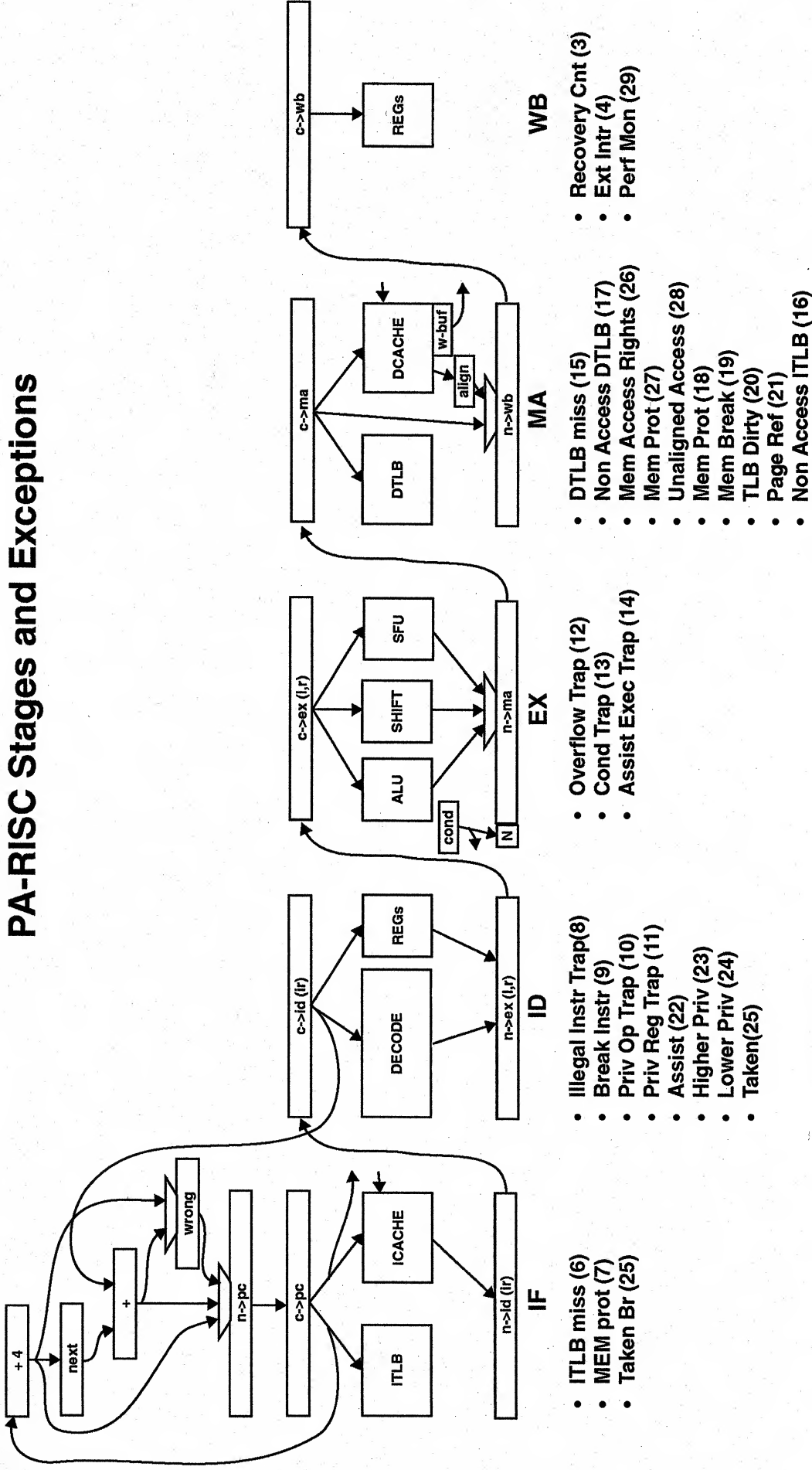


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PA-RISC Stages and Exceptions



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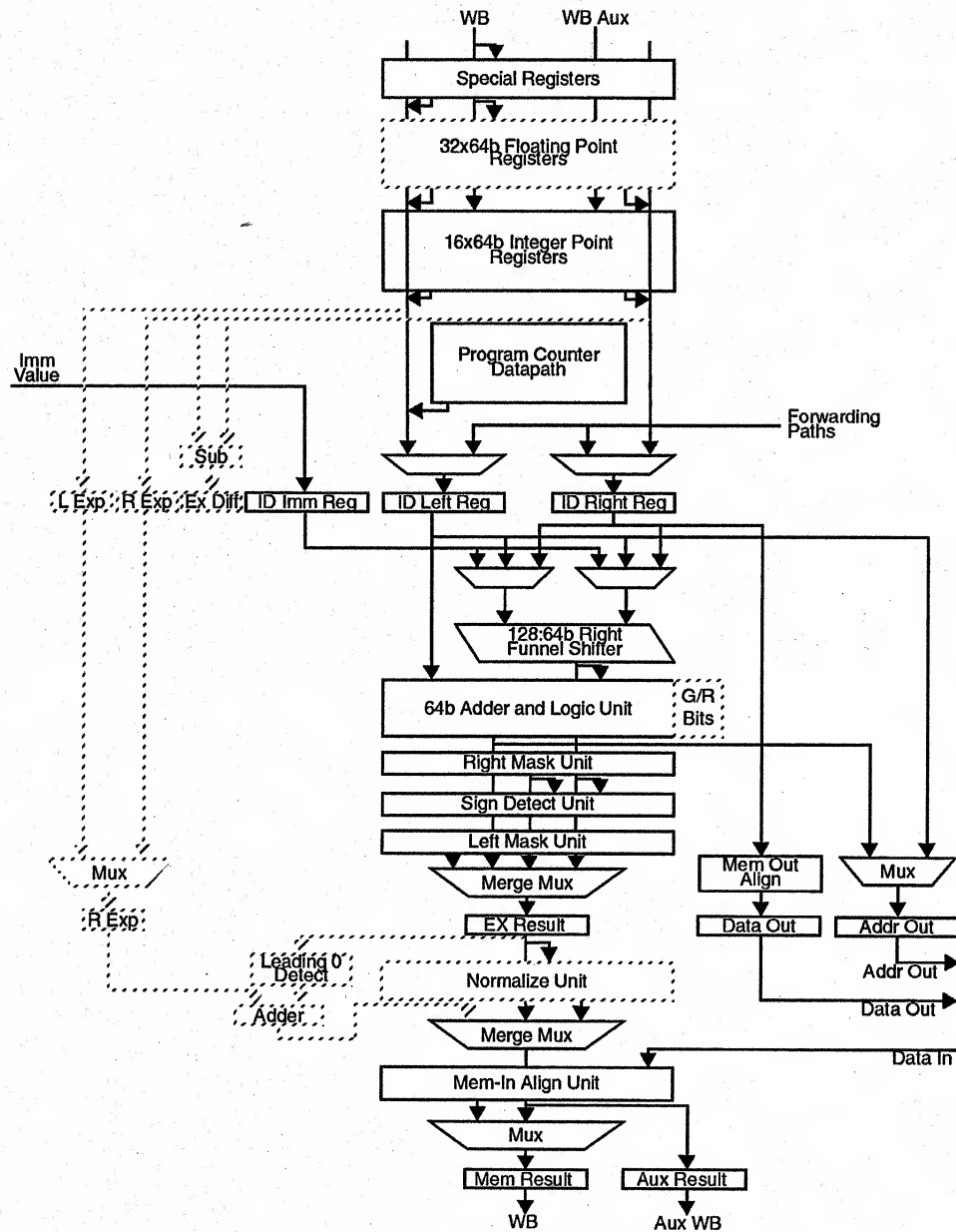
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Internal PA-RISC Datapath



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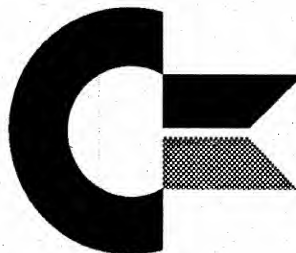
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PA-RISC MMU Implementation

- **Level 1 Implementation**
 - 16-bit space registers
- **Separate ITLB and DTLB**
 - **ITLB:**
 - 2 Block Entry (Operating System Code, Shared Libraries)
 - 8 Page Entries
 - **DTLB:**
 - 2 Block Entries (Frame Buffers)
 - 8 Page Entries

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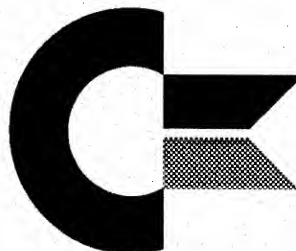
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PA-RISC Cache Implementation

- **Separate Instruction and Data Caches**
- **Both:**
 - 2-way set associative
 - 32-byte line size (4 64-bit accesses per line)
- **Data Cache:**
 - 32 lines (1 Kbytes) (Hope to increase to 64 lines (2 Kbytes))
 - Write-back storage policy
 - 1 line write buffer
- **Instruction Cache:**
 - 64 lines (2 Kbytes) (Hope to increase to 128 lines (4 Kbytes))

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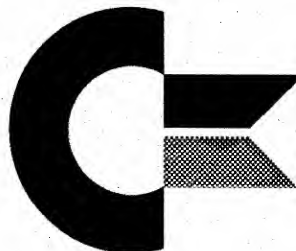
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PA-RISC Extensions

- **SFU Instructions to support:**
 - **Graphics**
 - **Graphics coordinate manipulation**
 - **Shading inner-loop manipulation of 5-5-5 pixels**
 - **Outcode clipping support**
 - **CD-ROM error correction**
 - **64-bit accesses**
- **Combined Integer/Floating Point support:**
 - **Necessity?**
 - **Support for emulation?**

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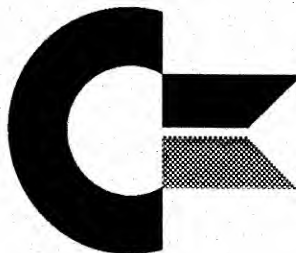
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Hombre SFU Instructions

GR_ARITH_5

04	r2	r1	01	3	sfu=1	0	rt
6	5	5	5	2	3	1	5

GR_ARITH_8

04	r2	r1	03	3	sfu=1	0	rt
6	5	5	5	2	3	1	5

GR_ARITH_5_5

04	r2	r1	02	3	sfu=1	0	rt
6	5	5	5	2	3	1	5

GR_ARITH_8_8

04	r2	r1	04	3	sfu=1	0	rt
6	5	5	5	2	3	1	5

GR_CLIP_SUB

04	r2	r1	05	3	sfu=1	0	t
6	5	5	5	2	3	1	5

GR_TEST

04	0	0	06	3	sfu=1	1	x
6	5	5	5	2	3	1	5

GR_MTCL

04	r2	00	07	3	sfu=1	0	0
6	5	5	5	2	3	1	5

GR_PACK_5_5

04	r2	00	08	3	sfu=1	0	t
6	5	5	5	2	3	1	5

GR_PACK_8_8

04	r2	00	09	3	sfu=1	0	t
6	5	5	5	2	3	1	5

GR_LDDX

0B	b	x	s	u	0	cc	0	uid=1	m	t
6	5	5	2	1	1	2	1	3	1	5

GR_STDX

09	b	x	s	u	0	cc	1	uid=1	m	r
6	5	5	2	1	1	2	1	3	1	5

GR_LDDS

0B	b	im5	s	a	1	cc	0	uid=1	m	t
6	5	5	2	1	1	2	1	3	1	5

GR_STDS

09	b	im5	s	a	1	cc	1	uid=1	m	r
6	5	5	2	1	1	2	1	3	1	5

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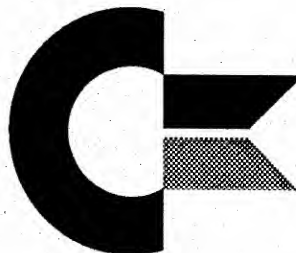
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Blitter

- **General**
 - Operates on 8, 16, or 24(32) bit pixels
 - All control registers (except function) are shadowed
 - Uses plane mask
 - Uses burst mode for faster accesses
 - Uses intelligent RMW cycles for faster accesses
 - Transparency mode permits easy insertion
- **Rectangular Blits**
 - Combines 0, 1, or 2 sources with destination rectangle
 - Uses one of 256 Boolean Functions
 - Forward and Reverse fetching
- **Expands**
 - 1:8, 1:16, 1:24(32) expands
 - Clipping optional
- **Line Draws**
 - Uses Bresenham algorithm
 - Pattern Register permits patterned lines
 - Clipping optional
- **Fills**
 - Shading is performed using fixed-point arithmetic
 - Texture mapping also uses fixed-point arithmetic
 - Clipping optional

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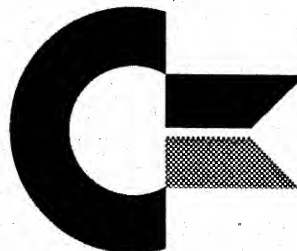
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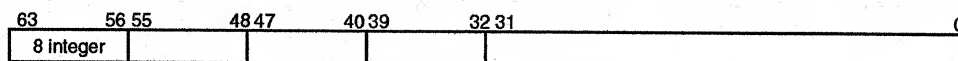
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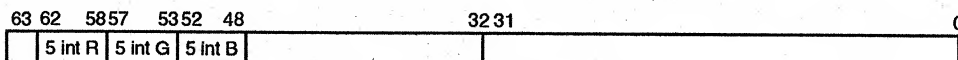
Pixel Data Types

- **During Display:**

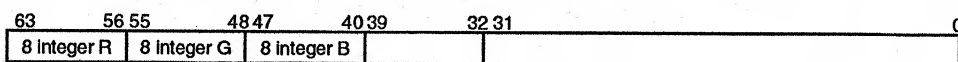
- **8-bit palette, HAM8:**



- **16-bit RGB (Hi-color):**

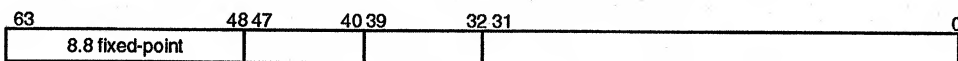


- **24(32)-bit RGB (True-color):**

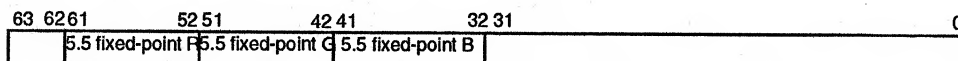


- **During Calculations:**

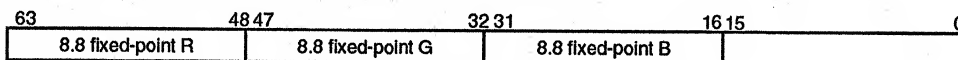
- **8-bit palette:**



- **16-bit RGB (True-color):**



- **24(32)-bit RGB (True-color):**



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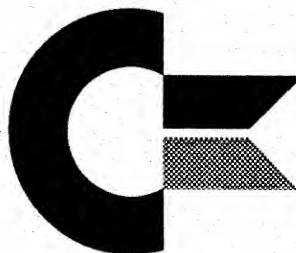
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